REMARKS

Reconsideration and allowance are respectfully requested in light of the above amendments and the following remarks.

Claims 11-14 have been amended to overcome the rejections under 35 USC §112, second paragraph.

Claims 14 and 6 were rejected under 35 USC §102(b) as being anticipated by Pfiester (US 4,918,510). Claims 13 and 5 were rejected under 35 USC §103(a) as being unpatentable over Pfiester in view of Nagatomo et al. (US 5,164,806). Claims 11, 12, 7, and 8 were rejected under 35 USC §103(a) as being unpatentable over Pfiester in view of Nagatomo and further in view of Murakami (U.S. 4,819,045). The Applicant respectfully traverses.

Anticipation Rejection of Claim 14 and Claim 6 Dependent Therefrom

It is well-settled that anticipation exists only if every element of the claimed invention, as arranged in the claim, is disclosed either expressly or inherently by a single prior art reference. *See Minnesota Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 1565 (Fed.Cir.1992); *Lindemann Maschinenfabrik GMBH, v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458 (Fed.Cir.1984). The identical invention must be shown in as complete detail as is contained in the claim.

Richardson v. Suzuki Motor Co., 868 F.2d1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Further, if an allegation of inherent anticipation is made by the Office, MPEP 2112 requires that it be supported by a *prima facie* case providing "objective evidence" or "cogent technical reasoning" tending to show that the allegedly inherent subject matter is *necessarily*, and not merely *possibly*, present in the cited reference.

It is submitted that the applied prior art neither expressly nor inherently discloses the subject matter of the present claims.

Claim 14 now recites:

> *A semiconductor device comprising:*
> *a source side offset diffusion layer region and a drain side offset diffusion layer region of a second conductivity type in a transistor formed, so as to be separated from each other, in a predetermined region in a region of a first conductivity type in a semiconductor substrate;*
> *a gate insulator film formed between said source side offset diffusion layer region and said drain side offset diffusion layer region;*
> *a gate electrode formed on said gate insulator film; and*
> *a diffusion layer of the first conductivity type of which an impurity concentration is higher than that of said region of the first conductivity type and which is formed so as to surround said source side offset diffusion layer region, said drain side offset diffusion layer region and said gate insulator film, wherein*
> *both ends of said gate insulator film in a channel width direction form protruding portions that protrude at borders of said source side offset diffusion layer region and of said drain side offset diffusion layer region in a direction toward said diffusion layer of the first conductivity type so that said protruding portions of said*

gate insulator film make direct contact with said gate electrode, and wherein

said diffusion layer of the first conductivity type is formed so as to surround said protruding portions and so as to be separated from the protruding portions by a predetermined distance.

Claim 14 is drawn to a structure having a diffusion layer of a first conductivity type: (1) surrounding protruding portions of a gate insulator film that make direct contact with a gate electrode, and (2) separated from the protruding portions by a predetermined distance. This structure provides an advantage in that an area of contact between the inversion layer, formed beneath the protruding portions of the gate insulator film, and the diffusion layers of the first conductivity type is reduced. As a result, a leakage current developed in the inversion layer of the semiconductor substrate, when a voltage is applied to the gate electrode via the protruding portions of the gate insulator film, can be reduced or prevented so that the transistor's breakdown voltage may be increased and its power consumption reduced. A description of how the leakage current develops in a related art device lacking the claimed features is provided in the specification on pages 3 and 4.

The Office Action states that Pfiester discloses a semiconductor device having protruding portions 54 formed at both ends of a gate insulator film 48 region, in the channel width

direction (Office Action, page 3, lines 6-7). These protruding portions 54 protrude at the borders of source and drain side offset diffusion layer regions 44 and 42, respectively, in a direction toward a diffusion layer 40 of a first conductivity type (Office Action, page 3, lines 7-9). Diffusion layer 40 is formed to surround protruding portions 54 and to be separated from them by a predetermined distance (Office Action, page 3, lines 9-12).

However, one of ordinary skill in the art of semiconductor technology would recognize the direction in which the semiconductor's drain 42, gate 46, and source 44 are aligned, as illustrated in Pfiester's Fig. 3, is defined as the channel length. One skilled in the art would also recognize the direction perpendicular to the channel length is defined as the channel width. The attached Exhibit entitled "Modern MOS Technology: Processes, Devices, and Design" elucidates this structural relationship.

As may be determined by inspection of Pfiester's Fig. 1 and its accompanying description, Pfiester's Fig. 1 is rotated counter-clockwise 90 degrees from the corresponding illustration provided by Applicant's Fig. 1A. Applicant's Fig. 1B is a cross-sectional view along line I-I' of Fig. 1A, and Pfiester's Fig. 3 is a cross-sectional view along line 3-3 of Fig. 1. Moreover,

Applicant's cross-sectional view along line I-I' cuts across the width of the illustrated semiconductor, whereas Pfiester's cross sectional view cuts along the length of the illustrated semiconductor.

Due to the cross-sectional view along the width of the semiconductor, illustrated by Applicant's Fig. 1B, the width-wise proportionality of the claimed features may be viewed in this illustration. Applicant's Fig. 1C shows another cross-sectional view along the line II-II' of Fig. 1A. A portion of this cross-sectional view, denoted by line S, is cut along the length of the semiconductor. As may be determined by examination of Fig. 1C, the width-wise proportions of the semiconductor features along the length-wise portion of the cross-sectional cut, line S, may not be seen from this perspective view. For example, looking only at line S in Fig. 1C, it is impossible to see the protrusion of the gate oxide film with respect to the borders of the source and drain diffusion layers.

The width-wise proportions of Pfiester's semiconductor features are impossible to determine in the length-wise cross-sectional view illustrated by Fig. 3. Since the cross-sectional view cut length-wise does not illustrate the width-wise proportionality of the semiconductor features in a, it follows that Pfiester's Fig. 3 cannot disclose the claimed gate insulator

film having protruding portions at both ends, in a channel width direction, that protrude at borders of the source and drain side offset diffusion layer regions in a direction toward the diffusion layer of the first conductivity type to make direct contact with a gate electrode.

Moreover, Pfiester's Fig. 3 discloses the gate insulator films of protruding portions 54 make contact with the drain and source regions 50 and 52, respectively. Protruding portions 54, as identified in the Office Action, of gate insulator 48 do not make contact with the gate electrode, only gate insulator 48 makes contact with the gate electrode. Accordingly, an inversion layer is not created in the semiconductor substrate, by a voltage applied to the gate electrode, in Pfiester's protruding portions 54, as occurs in the claimed protruding portions of the gate insulator film. As a result, Pfiester's structure does not prevent leakage current between an inversion layer and the diffusion layers.

In accordance with the above discussion, the Applicant respectfully submits that Pfiester does not anticipate the features of present claim 14. Specifically, Pfiester fails to disclose at least the claimed gate insulator film having protruding portions at both ends, in a channel width direction, that protrude at borders of the source and drain side offset

diffusion layer regions in a direction toward the diffusion layer of the first conductivity type to make direct contact with a gate electrode. Therefore, allowance of claim 14 and claims 6, 8 and 12 dependent therefrom is warranted.

Obviousness Rejection of Claim 13 and Claims Dependent Therefrom

The Office Action states that Pfiester discloses the entire structure of claim 13, except for a diffusion layer formed in contact with protruding portions of a gate insulator film (Office Action, page 4, lines 1-5). Nagatomo is cited in the Office Action for a teaching of forming the diffusion layer in contact with the protruding portions.

Claim 13 recites the same features discussed above in connection with the rejection of claim 14. For the same reasons that claim 14 is patentable over Pfiester's semiconductor device, claim 13 is similarly patentable.

Moreover, Nagatomo does not cure the deficiencies of Pfiester. Nagatomo discloses a low concentration p— impurity region 15 formed between a high concentration n+ impurity region 5a and a high concentration channel stop layer 8. With this structure, the breakdown voltage of the junction around region 5a can be increased. However, the technology of Nagatomo, as described in column 12, lines 1 to 7, is based on a technical

idea wherein the depletion layer is expanded to relieve the electrical field through the formation of low impurity concentration region 15. Thereby, the breakdown voltage of the PN junction of 5a is increased.

By contrast to the teaching of Nagatomo, the present claimed invention is based on a technical idea wherein the inversion layer formed beneath the protruding portions of the gate insulator film does not overlap the diffusion layers, which correspond to Nagatomo's channel stops, but merely makes contact with them so that the area of contact of the inversion layer and the diffusion layers is reduced. This provides advantages that leakage current is prevented and the semiconductor's breakdown voltage is increased.

In other words, the technical ideas for increasing the breakdown voltage in Nagatomo and in the present claimed invention are significantly different. Nagatomo does not teach reducing the leakage current by reducing the area of contact between the inversion layer and the diffusion layers, as taught by Applicant.

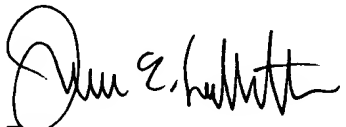
Accordingly, Nagatomo does not provide the motivation to modify the semiconductor device taught by Pfiester to produce the claimed invention and provides no reasonable expectation of success in so modifying Pfiester's device. Therefore, allowance

of claim 13 and all claims depending therefrom is warranted for this independent reason.

In view of the above, it is submitted that this application is in condition for allowance and a notice to that effect is respectfully solicited.

If any issues remain which may best be resolved through a telephone communication, the Examiner is requested to telephone the undersigned at the local Washington, D.C. telephone number listed below.

Respectfully submitted,



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